Page 64, third full paragraph, replace with the following:

In Embodiment 7 the second syndrome calculator 52 and the second error detector 72 process demodulated data only. In this case, while the second syndrome calculator 52 is performing syndrome calculation for demodulated data (a code word) one time, the first syndrome calculator 51 executes syndrome calculation for data in the buffer memory 4 twice. Thus, if these syndrome calculators have an equal capacity, the second syndrome calculator 52 will stand idle for some time.

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IN THE CLAIMS:

Please amend claims 9-12, 16, 20, 24 and 31 as follows:

9. (Amended) The error correction device of claim 7 further comprising a storing means for storing mid-term results, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means until said syndrome calculating means detects an error-containing code, wherein

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said non-error range designating sub means is a non-error sector code word range designating sub means for designating, in code word units of a sector, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing code and on said information that designates the position of the error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of the sector from which an error-containing code has been detected, based on the information designated by said non-error sector code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said storing means as an initial value.

10. (Amended) The error correction device of claim 7 further comprising a sector-basis storing means for storing mid-term results, on a sector-by-sector basis, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means, until said syndrome calculating means detects an error-containing code, wherein

said non-error range designating sub means is a sector-basis non-error code word range designating sub means for designating, on a sector-by-sector basis, in code word units, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing code and on said information that designates the position of the error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of each sector from which an error-containing

code has been detected, based on the information designated by said sector-basis non-error code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said sector-basis storing means as an initial value.

11. (Amended) The error correction device of claim 7 further comprising a sector-group-basis storing means for storing mid-term results, on a sector-group-by-sector-group-basis, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means until said syndrome calculating means detects an error-containing code, wherein

said non-error range designating sub means is a sector-group-basis non-error code word range designating sub means for designating, on a sector-group-by-sector-group-basis, in code word units, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that

designates the code word including the error-containing code and on said information that designates the position of the error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of each sector group from which an error-containing code has been detected, based on the information designated by said sector-group-basis non-error code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said sector-group-basis storing means as an initial value.

12. (Amended) The error correction device of claim 1, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal

direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

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said system control means comprises:

a means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory done by said bus control means; for recognizing an ECC block in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

an ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

16. (Amended) The error correction device of claim 1, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

Q12 said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

an means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said ECC-block-basis buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-

numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means in said system control means recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the code words which are to be processed therein.

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20. (Amended) The error correction device of claim 1, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

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said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data

to said plural-ECC-block-division buffer memory by said bus control means; for recognizing ECC blocks in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

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24. (Amended) The error correction device of claim 1, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a

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parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

a14 said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage

known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC

blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

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31. (Amended) The error correction device of claim 1, further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

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an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.